

PRANAV VINOTH

RTL Design | FPGA | Embedded Systems

Seeking Summer 2027 Internship in Digital Design, Verification, and FPGA

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TECHNICAL SKILLS

Hardware & Verification: RTL Design, SystemVerilog, Verilog, UVM, FSM Design, Testbench Development, Regression Testing, Debugging, AMD Vivado, AMD Vitis, AXI, KiCad

Software: C, C++, Python, Java, Git, Linux, PyTorch (CUDA)

Simulation & Test: LTspice, SiMetrix SPICE, Digilent Waveforms, Oscilloscope, Logic Analyzer

Platforms: AMD Zynq-7000 SoC FPGA, ARM Cortex-A9, ESP32, Raspberry Pi

EDUCATION

B.S. Electrical and Computer Engineering, Minor in Quantum Engineering

Expected May 2028

University of Colorado Boulder | Boulder, CO | Major GPA: 3.15

Coursework: Digital Logic, Programming Digital Systems, Microelectronics, Programming Embedded Systems, Electronics Design Lab, Advanced Circuit Analysis

PROJECTS

RV32IM RISC-V CPU with HDMI Video Controller (Arty Z7-20)

Fall 2026

Verilog, Vivado, RISC-V ISA, HDMI/TMDS

- Designed a **multi-cycle RV32IM RISC-V processor** in Verilog with a fetch, decode, execute, memory, writeback FSM
- Built a **self-checking Verilog testbench and 88-case assembly test plan** covering the RV32I base ISA and M extension, including divide-by-zero and overflow edge cases
- Automated an **assembly-to-hex-to-simulation regression flow** with timeout detection and per-test pass/fail reporting
- Built a **640x480 HDMI controller** with TMDS encoding and a CPU-writable frame buffer in one 125 MHz clock domain, using a divide-by-5 pixel clock enable to avoid clock domain crossing; demoed Snake on hardware

Ethernet MAC Byte-Stream Parser (Arty Z7-20)

Summer 2025

SystemVerilog, UVM, C, Vivado, AMD Zynq-7000 SoC

- Wrote bare-metal C on the Zynq ARM core to pass Ethernet frames over AXI to a SystemVerilog byte-stream parser
- Measured 150 μ s end-to-end latency** from PHY to parsed output, extracting payloads from 80-byte frames
- Built a **UVM environment with an agent (sequencer, driver, monitor) and scoreboard** to verify parser frame handling

Two-Layer USB-C Phone Charger PCB

Spring 2025

KiCad, PCB Layout, DC-DC Power Conversion, USB-C

- Designed a **two-layer PCB in KiCad** for a portable phone charger with a boost converter, battery pack, and USB-C output rated up to 60W for iPhone fast charging

EXPERIENCE

Machine Learning Researcher

May 2026 - Present

BOLD Lab, University of Colorado Boulder | Boulder, CO

- Predicted magnetic core loss at 4.78% error across 4 unseen materials** using BelNet and DeepONet models in PyTorch, from excitation waveform, frequency, and temperature

AWS Engineer Intern

May 2025 - Aug 2025

Exterro | Coimbatore, India

- Deployed AWS EC2 instances and S3 buckets, managed over SSH on Linux, to store and process document datasets

ML Engineer Intern

May 2024 - Aug 2024

Exterro | Frisco, TX

- Cut document review time by 60%** with a TensorFlow classifier sorting files by type (91% accuracy, 50K+ docs)

AWARDS

1st Place, IEEE Region 5 Student Hardware Competition, Circuit Design Category

Feb 2026

Designed the ESP32 sensor circuit (temperature, humidity, CO₂, CO, sound level) and co-developed a live multi-device web dashboard; 1st of 26 teams (20+ universities), judged by industry and IEEE professionals on sensor accuracy and presentation